

EXPERIMENT 2

Inverting Logic: NOT, NAND, & NOR

OBJECTIVES:

- Examine inverting logic circuits.
- Demonstrate the characteristics of NOT, NAND, and NOR gates.
- Develop truth tables for NOT, NAND, and NOR gates.

MATERIALS:

- Xilinx Vivado software, student or professional edition V2018.2 or higher.
- IBM or compatible computer with Pentium III or higher, 128 M-byte RAM or more, and 8 G-byte Or larger hard drive.
- BASYS 3 Board.

DISCUSSION:

The inverter (or NOT gate) represents logical complementation. A NOT gate can have only one input and one output. The output of a NOT gate simply reverses (inverts) the logic value presented at its input. The NOT gate can be combined with AND and OR gates to construct two more basic gates: NAND and NOR gates. Both NAND and NOR gates are universal logic gates, which means that either NAND gates or NOR gates can be used to construct any combinational logic circuit. We will use gate symbols, truth tables, and Boolean equations to demonstrate their characteristics. As with AND and OR gates, NAND and NOR gates can have two or more inputs but only one output.

Gate Characteristics:

1. The NOT Gate

Symbol	Boolean Equation	Truth Table
A - D- X	$\mathbf{X} = \mathbf{A}$	InputOutputAX0110

Because the NOT gate has only one input, the truth table has two rows. Moreover, the output inverts the logic level of the input. In addition to the overhead bar shown above (read as "X = A-bar'), notation for logical inversion includes the following:

Symbol **Truth Table Boolean Equation** Inputs Output Y B А Y Y = AB0 0 1 В 0 1 1 0 1 1 0 1 1 Page 2 | 19

2. The NAND Gate

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The behavior of a NAND gate can be summarized as follows: The output is LOW only when all the inputs are HIGH. If one or more inputs are LOW (false or logic 0), the output will be HIGH. Comparing the truth table for the NAND gate with that of the AND gate, you will find out that each output of a NAND gate is exactly the opposite (inverted) logic value of the corresponding output of an AND gate. In fact, a NAND gate is functionally equivalent to an AND gate cascaded with a NOT gate as shown below.



Symbol	Boolean Equation	Truth Table
$B^{A} \longrightarrow Z$	Z = A + B	Inputs Output A B Z 0 0 1 0 1 0 1 0 0 1 1 0

As seen from the above truth table, the output of a NOR gate is HIGH only when *all* the inputs are LOW. If one or more of the inputs are HIGH, then the output is LOW. Similarly, a NOR gate can be constructed using an OR gate cascaded with a NOT gate. In other words, a NOR gate is functionally equivalent to an OR gate followed by an inverter.



3. The NOR Gate

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In the later part of this experiment, we will show how NAND and NOR gates can be used to perform some useful functions such as enabling and disabling signals. Also, we will show how to use NAND and NOR gates to perform the function of a NOT gate.

PROCEDURE:

1. Open Xilinix Vivado.

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2. In the Xilinx-Project Navigator window, Quick start, New Project.

New Project	
	Create a New Vivado Project
HLx Editions	This wizard will guide you through the creation of a new project.
	To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a default part.
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3. Name the project.

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4. Choose "RTL Project" and check the "Do not specify sources at this time" as we will configure all the settings manually through the navigator from inside the project.

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\bigcirc	Imported Project Create a Vivado project from a Synplify, XST or ISE Project File.		
\bigcirc	Example Project Create a new Vivado project from a predefined template.		
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5. Select New Source... and the New window appears. In the New window, choose Schematic, type your file name (such as *source_1*) in the File Name editor box, click on OK, and then click on the Next button.

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7. The Define Module Window that will appear, we will choose the input and output labels for the gates under investigation in this experiment. In this experiment, we are investigating a 3-input NAND gate and 3-input NOR and a NOT (Inverse) gate. Then Under "Port Name", add "A0", "A1", "A2" as inputs for NAND gate, add "B0", "B1", "B2" as inputs for NOR gate and add "C", as inputs for the NOT gate. Then add "X", "Y", "Z" as outputs for the mentioned gates and select OK.

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8. In the "source_1.vhd" created file, type the gates equivalent VHDL code for the NAND, NOR and NOT gates between the "begin" and "end Behavioral" as follows and then save the file.

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9. Next, we need to add To add a constraint file with the".xdc" extension, as following: Go to "Flow Navigator" and from "Project Manager" select "Add Sources" then "Add or create constraints". Next, choose "Create File" and enter the file name "lab_2" then "OK" followed by "Finish".

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- 10. Then, we need to get a template xdc file that is going to be edited according to the different experiments. Google "basys 3 xdc file" and choose the "xilinix" link that appears (<u>https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/Basys3/Supporting%20Material/Basys3_Master.xdc</u>). Copy the whole file and paste it into the "lab_2.xdc" that you have just created in the last step. Then uncomment and edit the input Switches and the output LEDs as in the next step.
- 11. Uncomment (by deleting the # sign) sw[0], sw[1], sw[3],.... led[0], led[1],...
 lines. Note that each of them has two successive lines (Uncomment both of them). Do the following replacements: sw[0] → A0, sw[1] → A1,...., led[0] → X, led[1] → Y,..., then Save the file

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ilinx/Vivado/2018.2/project/project.srcs/constrs_1/new/lab_2.xdc	>
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#set property IOSTANDARD LVCMOS33 [get ports clk]	
<pre>#create_clock -add -name sys_clk_pin -period 10.00 -waveform {0 5} [get_ports clk]</pre>	
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<pre>7 #set_property PACKAGE_PIN W5 [get_ports clk] 8 #set_property IOSTANDARD LVCMOS33 [get_ports clk] 9 #create_clock -add -name sys_clk_pin -period 10.00 -waveform (0 5) [get_ports clk] 10 11 ## Svitches 12 set_property PACKAGE_PIN V17 [get_ports [A0]] 13 set_property IOSTANDARD LVCMOS33 [get_ports [A0]] 14 set_property PACKAGE_PIN V16 [get_ports [A1]] 15 set_property PACKAGE_PIN V16 [get_ports [A1]] 16 set_property IOSTANDARD LVCMOS33 [get_ports [A1]] 17 set_property IOSTANDARD LVCMOS33 [get_ports [A2]] 18 set_property IOSTANDARD LVCMOS33 [get_ports [A2]] 19 set_property PACKAGE_PIN W16 [get_ports [B0]] 20 set_property IOSTANDARD LVCMOS33 [get_ports [B1]] 21 set_property PACKAGE_PIN W15 [get_ports [B1]] 22 set_property IOSTANDARD LVCMOS33 [get_ports [B1]] 23 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 24 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 25 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 26 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 27 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 28 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 29 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 20 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 20 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 23 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 24 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 25 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 26 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 27 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 28 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 29 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 29 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 20 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 29 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 20 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 29 set_property IOSTANDARD LVCMOS33 [get_ports [B2]] 20 s</pre>	
<pre>24 set_property PACKAGE_PIN %14 [get_ports [C]] 25 set_property DOSTANDARD UVCMOS33 [get_ports [Sv[7]]) 26 #set_property DOSTANDARD UVCMOS33 [get_ports [sv[7]]] 27 #set_property IOSTANDARD UVCMOS33 [get_ports [sv[7]]] 28 #set_property PACKAGE_PIN vg [get_ports [sv[8]]] 30 #set_property PACKAGE_PIN vs [get_ports [sv[8]]] 31 #set_property PACKAGE_PIN vs [get_ports [sv[8]]] 32 #set_property PACKAGE_PIN vs [get_ports [sv[9]]] 33 #set_property DOSTANDARD UVCMOS33 [get_ports [sv[9]]] 34 #set_property PACKAGE_PIN vs [get_ports [sv[10]]] 35 #set_property PACKAGE_PIN vs [get_ports [sv[10]]] 36 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 37 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 38 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 39 #set_property DOSTANDARD UVCMOS33 [get_ports [sv[11]]] 30 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 31 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 32 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 33 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 34 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 35 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 35 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 36 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 37 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 38 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 39 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 30 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 30 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 31 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 32 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 33 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 34 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 35 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 36 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 35 #set_property PACKAGE_PIN vs [get_ports [sv[11]]] 36 #set_property</pre>	

12. From the tool tab choose the play button and then "Run Implementation". Select "Number of jobs" =1 and then press OK.

🔥 Launch Runs	×
Launch the selected synthesis or implementation runs.	4
Launch directory: See <default directory="" launch=""></default>	~
Options	
● Launch runs on local host: Number of jobs: 1 ~	
◯ <u>G</u> enerate scripts only	
Don't show this dialog again	
OK Cance	I

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13. The implementation errors window will appear if any or the successfully completed window. From this window select "Generate Bitstream" and then OK. This will make the software generate ".bin" file to be used in programing the hardware BAYAS 3.

Implementation Completed			
Implementation successfully completed.			
Open Implemented Design			
Generate Bitstream			
O View Reports			
Don't show this dialog again			
OK Cancel			

14. The next window will appear in which choose "Open Hardware Manger", connect the Hardware Kit to the USB port and then press OK.

Bitstream Generation Completed	×	
Bitstream Generation successfully completed.		
Open Implemented Design		
◯ <u>V</u> iew Reports		
• Open <u>H</u> ardware Manager		
O Generate Memory Configuration File		
Don't show this dialog again		
OK Cancel		
AP21.		
	P a	ge 13

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15. A green tab will appear in the top of the Vivado window, from which choose "open target" to program the hardware.

HARDWARE MNIAGER - unconnected ?				
No hardware target is open. Open target				
Hardware ? _ D E ×	source_1.vhd × lab_2.xdc ×	2 0 0		
$\mathbb{Q}_{1} \mid \stackrel{\times}{=} \mid \stackrel{\otimes}{=} \mid \stackrel{\circ}{=} \mid \stackrel{\circ}{=} \mid \stackrel{\circ}{=} \mid \stackrel{\circ}{=} \mid \stackrel{\otimes}{=} \mid \stackrel{\otimes}{=} \mid \stackrel{\otimes}{=} \mid \stackrel{\circ}{=} \mid {=} \mid {=} \mid }{=} \mid }}$	C://ilinu/l/vado/2018.2/project/project.srcs/sources_1/new/source_1.vhd	×		
		٠		
No content	27use IEEE.NUMBERC_STD.ALL; 28 Uncomment the following library declaration if instantiating 30	~		
Source File Properties ? _ D 🗹 ×	40 B2 : in sm_looic. 40 B2 : in sm_looic.			
● source 1.vhd ← → ✿	41 C : in STD_LOGIC; 42 X : out STD LOGIC;			
Enabled Location: C.Xtlimx/lvado/2018.2/project/project. Type: VHDL Library: di_defaultiib Size: 1.3 KB Modified: Today at 16.27.53 PM	43: Y: out STD_LODIC; 44: 2: out STD_LODIC; 45: end source_l: 47: architecture Behavioral of source_l is 48: i 49: begin 50: X << (AD HND A1) HAND A2;3 input HAND Gate			
Ceneral Properties	55	~		

16. From the window appears, select the ".bin" file from the Project you create by browsing for the generated ".bit file" under the ".runs" folder and program the board then press OK.

Look <u>i</u> n:	impl_1	✓ ♠☆⊋±À险ХС 🏢
.Xil		Recent Directories
B source_1	1.bit	C:/Xilinx/Vivado/2018.2
		File Preview
		File:source_1.bit Directory: C.XIIInvWado/2018.2/project/project.runs/impl_1 Created:Today at 16:31 PM Accessed:Today at 16:31 PM Modified: Today at 16:31 PM Store: 2.1 MB Type: Bistream file Owner: ECE-3865-832Ftmabde030
le name:	source 1.bit	
es of type:	- Bitstream Files (bit bin rbt)	
		СК Салс

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17. Notice that the 7-segment on the hardware is counting up from 0 to 9 frequently until you download the program and it will stop.



18. Fill in the following truth tables for all the gates by observing the inputs/outputs on the programmed board.

A. NAND Gate

Truth Table (1)

A0	A1	A2	X
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

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B. NOR Gate

Truth Table (2)

BO	B1	B2	Y
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

Symbol

Boolean Equation

a. NOT Gate

Truth Table (3)

0	
1	

Symbol Boolean Equation

 Boolean Equation

 Boolean Equation

 Boolean Equation

 Boolean Equation

Experiment 2

Logic Design L	ab EEL3712I	Experiment 2
19.	Verify that the experimental results are consistent with the Discussion	on.
Checked by_	Date	
	Ρ	age 18 19

Questions:

- 1. Create a Xilinx project called *LAB2* in the same way that you did the projects *AND_OR3* and *INVERT* In this new project prove the following:
- a) A 2-input NAND gate is equivalent to a 2-input AND gate followed by a NOT gate.
- b) A 2-input NOR gate is equivalent to a 2-input OR gate followed by a NOT gate.
- c) A 2-input NAND gate is equivalent to an inverter when the two inputs are tied together.
- d) A 2-input **NOR** gate is equivalent to an inverter when one of the inputs is connected to ground.
 - 2. Draw the truth tables in the following to demonstrate your results obtained in the last step. Do they match what you expected?